深圳市盛思达通讯技术有限公司

RK3288 核心板规格书
规格型号：S219_V1.0

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目录

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1. 概述

S219 核心板采用了瑞芯微 RK3288 四核处理器，其 CPU 采用 Cortex-A17 构架设计，频率高达 1.8GHz，GPU 集成 ARM 的 Mali-T764。

S219 核心板适用于广告展示终端、工业设备控制、电子支付设备、电子自助终端等高稳定性要求行业，尤其适合应用于需要进行人机交互界面的场景应用。

S219 核心板接口非常丰富，可以适配大部分的行业需求。可以根据不同的使用场景灵活的设计底板，可快速灵活的运用于各行各业。

2. 主要技术参数

CPU	超强四核 Cortex-A17，频率高达 1.8GHz
GPU	ARM Mali-T764 GPU，支持 TE，ASTC，AFBC 技术
内存	DDR3 标贴 2GB，最高支持 4GB
存储	EMMC FLASH 8GB/16G/32G 可选，标贴 8GB；支持 SATA 硬盘接口，TF 卡最大支持 32GB
操作系统	Android 5.1
电源输入	3.7~5.5V(推荐使用 5V 输入)
显示接口	1 x HDMI 2.0 ，支持 4K@60 帧输出 1 x MIPI、1 x EDP、2 x LVDS 液晶屏显示接口
摄像头接口	1 x DVP 摄像头接口（最高支持 5Mpixel），1 x MIPI-CSI 摄像头接口 （最高支持 13Mpixel ）
触摸屏	提供 I2C 接口（可以支持多点电阻触摸，多点电容触摸）。支持 USB 多点红外触摸，多点电容触摸，多点纳米膜触摸，多点声波触摸，多点光学触摸。
网络	1 x RJ45 百兆/千兆以太网口
	WIFI 支持 2.4G/5G WIFI，支持 WI-FI802.11 a/b/g/n 协议
	蓝牙 V2.1+EDR/Bluetooth 3.0/3.0+HS/4.0
	3G/4G 功能，支持 LTE-TDD/LTE-FDD/TD-SCDMA/CDMA/EDGE/GPRS/GSM
接口设备	4 路串口，支持带流控串口
	4 路 I2C 接口
	2 x USB2.0 HOST，1 x USB2.0 OTG
	1 路 SPI 接口
	1 路 I2S 接口
	1 路 ADC 接口
	1 路 SDIO 输出通道
	3 个按键接口自定义

实时时钟	内置实时时钟供电接口，支持定时开关机
系统看门狗	支持软件，硬件看门狗
音频格式	MP3,WMA,WAV,APE,FLAC,AAC,OGG,M4A,3GPP 格式
视频格式	支持 H264，VP8，MAV，WMV,AVS,263,MPEG4 等视频格式的 1080P 多视频解码

3. 整体引脚说明

本模块采用邮票孔封装，一共有 216 个引脚。 模块各引脚的定义请参见下表：

Pin	Ball Pin Name	Pad type	IO Pull	Reset State	Default function	Defual function description	Function 2	IO Domain
1	VADP	P				DC 5V 电源输入脚		
2	VADP	P				DC 5V 电源输入脚		
3	VCC_BAT+	P				电池正极		
4	VCC_BAT+	P				电池正极		
5	NTC					电池温度检测脚		
6	VCC_BAT-	P				电池负极		
7	VCC_BAT-	P				电池负极		
8	MIPI_TX_D0P	A			MIPI_TX_D0P	MIPI-DSI differential lane 0 positive		MIPI_TX
9	MIPI_TX_D0N	A			MIPI_TX_D0N	MIPI-DSI differential lane 0 negative		
10	MIPI_TX_D1P	A			MIPI_TX_D1P	MIPI-DSI differential lane 1 positive		
11	MIPI_TX_D1N	A			MIPI_TX_D1N	MIPI-DSI differential lane 1 negative		
12	MIPI_TX_CLKP	A			MIPI_TX_CLKP	MIPI-DSI differential clock lane positive		
13	MIPI_TX_CLKN	A			MIPI_TX_CLKN	MIPI-DSI differential clock lane negative		
14	MIPI_TX_D2P	A			MIPI_TX_D2P	MIPI-DSI differential lane 2 positive		
15	MIPI_TX_D2N	A			MIPI_TX_D2N	MIPI-DSI differential lane 2 negative		
16	MIPI_TX_D3P	A			MIPI_TX_D3P	MIPI-DSI differential lane 3 positive		
17	MIPI_TX_D3N	A			MIPI_TX_D3N	MIPI-DSI differential lane 3 negative		
18	LCD_VDD	P				LCM power supply 3.3V 输出		LCDC0
19	LCDC0_HSYNC /GPIO1_D0	I/O	down	I	LCDC0_HSYNC	LCDC horizontal sync signal output		
20	LCDC0_VSYNC/ GPIO1_D1	I/O	down	I	LCDC0_VSYNC	LCDC vertical sync signal output		
21	LCDC0_DEN/G PIO1_D2	I/O	down	I	LCDC0_DEN	LCDC data enable		
22	LCDC0_DCLK/G PIO1_D3	I/O	down	I	LCDC0_DCLK	LCDC pixel clk output		
23	LCDC0_D23/LV DS_CLK1N	A			LCDC0_D23	LCDC data port	LVDS_CLK1N	LVDS
24	LCDC0_D22/LV DS_CLK1P	A			LCDC0_D22	LCDC data port	LVDS_CLK1P	

25	LCDC0_D21/LVDS_D9N	A			LCDC0_D21	LCDC data port	LVDS_D9N	
26	LCDC0_D20/LVDS_D9P	A			LCDC0_D20	LCDC data port	LVDS_D9P	
27	LCDC0_D19/LVDS_D8N	A			LCDC0_D19	LCDC data port	LVDS_D8N	
28	LCDC0_D18/LVDS_D8P	A			LCDC0_D18	LCDC data port	LVDS_D8P	
29	TRACE_CTL/LCDC0_D17/LVDS_D7N	A			LCDC0_D17	LCDC data port	LVDS_D7N	
30	TRACE_CLK/LCDC0_D16/LVDS_D7P	A			LCDC0_D16	LCDC data port	LVDS_D7P	
31	TRACE_D15/LCDC0_D15/LVDS_D6N	A			LCDC0_D15	LCDC data port	LVDS_D6N	
32	TRACE_D14/LCDC0_D14/LVDS_D6P	A			LCDC0_D14	LCDC data port	LVDS_D6P	
33	TRACE_D13/LCDC0_D13/LVDS_D5N	A			LCDC0_D13	LCDC data port	LVDS_D5N	
34	TRACE_D12/LCDC0_D12/LVDS_D5P	A			LCDC0_D12	LCDC data port	LVDS_D5P	
35	TRACE_D11/LCDC0_D11/LVDS_CLK0N	A			LCDC0_D11	LCDC data port	LVDS_CLK0N	
36	TRACE_D10/LCDC0_D10/LVDS_CLK0P	A			LCDC0_D10	LCDC data port	LVDS_CLK0P	
37	TRACE_D9/LCDC0_D9/LVDS_D4N	A			LCDC0_D9	LCDC data port	LVDS_D4N	
38	TRACE_D8/LCDC0_D8/LVDS_D4P	A			LCDC0_D8	LCDC data port	LVDS_D4P	
39	TRACE_D7/LCDC0_D7/LVDS_D3N	A			LCDC0_D7	LCDC data port	LVDS_D3N	
40	TRACE_D6/LCDC0_D6/LVDS_D3P	A			LCDC0_D6	LCDC data port	LVDS_D3P	
41	TRACE_D5/LCDC0_D5/LVDS_D2N	A			LCDC0_D5	LCDC data port	LVDS_D2N	
42	TRACE_D4/LCDC0_D4/LVDS_D2P	A			LCDC0_D4	LCDC data port	LVDS_D2P	
43	TRACE_D3/LCDC0_D3/LVDS_D1N	A			LCDC0_D3	LCDC data port	LVDS_D1N	
44	TRACE_D2/LCDC0_D2/LVDS_D1P	A			LCDC0_D2	LCDC data port	LVDS_D1P	
45	TRACE_D1/LCDC0_D1/LVDS_D0N	A			LCDC0_D1	LCDC data port	LVDS_D0N	
46	TRACE_D0/LCDC0_D0/LVDS_D0P	A			LCDC0_D0	LCDC data port	LVDS_D0P	
47	GND	G			GND			
48	ADC_IN2	I			HP_HOOK	耳机线控按键		
49	RECOVER	I			RECOVER	按键		
50	ADC_IN0	I			BAT_DET	Battery voltage input		
51	RTC_CLKOUT	O			RTC_CLKOUT	32KHz clock output		

52	RESET	I			RESET	system reset input		
53	PMIC_PWRON	I			PMIC_PWRON	system power key		
54	VCC_EFUSE	I			VCC_EFUSE	EFUSE power input (1.5V)		
55	VCC_RTC	I			VCC_RTC	RTC power input (1.7-3.5V)		
56	VCC_IO	O			VCC_IO	VCC_IO power output (3.3V)		
57	VCC_18	O			VCC_18	VCC_18 power output (1.8V)		
58	GND	G			GND			
59	VCC50_USB	I			VCC50_USB	USB power input(4.5V-5.5V)		
60	OTG_DM	A			OTG_DM	USB OTG Data Minus port		
61	OTG_DP	A			OTG_DP	USB OTG Data Plus port		
62	OTG_ID	A			OTG_ID	USB OTG ID detect input,need external pull-up		
63	GND	G			GND			
64	HOST1_DM	A			HOST1_DM	USB HOST1 Data Minus port.don't support USB1.1		
65	HOST1_DP	A			HOST1_DP	USB HOST1 Data Plus port.don't support USB1.1		
66	GND	G			GND			
67	HOST2_DM	A			HOST2_DM	USB HOST2 Data Minus port		
68	HOST2_DP	A			HOST2_DP	USB HOST2 Data Plus port		
69	GND	G			GND			
70	VCCIO_PMU	P			VCCIO_PMU	VCCIO_PMU power output (3.3V)		
71	VCC_TP	P			VCC_TP	VCC_TP power output (3.3V)		
72	DDRIO1_RETEN/PMUGPIO0_A3	I/O	up	I	EFUSE_PWR	EFUSE VPQS power control output		VCCIO_PMU
73	UART2_RX/IR_RX/PWM2/GPIO7_C6	I/O	up	I	UART2_RX	Uart2 serial port data input,for debug IR_RX	IR_RX	
74	UART2_TX/IR_TX/PWM3/EDPHDMI_CEC/GPIO7_C7	I/O	up	I	UART2_TX	Uart2 serial port data output,for debug	IR_TX	
75	GPS_MAG/HSADC_D0_T1/UART3_RX/GPIO7_A7	I/O	up	I	GPS_MAG		UART3_RX	
76	GPS_SIG/HSADC_D1_T1/UART3_TX/GPIO7_B0	I/O	down	I	GPS_SIG		UART3_TX	
77	GPS_RFCLK/GPS_CLK_T1/UART3_CTSn/GPIO7_B1	I/O	up	I	GPS_CLK		UART3_CTSn	
78	UART3_RTSn/GPIO7_B2	I/O	up	I	GPS_PWR	GPS power control output	UART3_RTSn	

79	PWM0/GPIO7_A0	I/O	down	I	LCD_BL	LCD panel backlight brightness control output		
80	PWM1/GPIO7_A1	I/O	down	I	PWM_LOG	PMIC power dynamic voltage scaling control,for LOG_PWM		
81	I2C4_SDA/GPIO7_C1	I/O	up	I	I2C4_SDA_TP	I2C serial port 4,for Touch panel,need external pull-up		
82	I2C4_SCL/GPIO7_C2	I/O	up	I	I2C4_SCL_TP	I2C serial port 4,for Touch panel,need external pull-up		
83	PS2_CLK/GPIO8_A0	I/O	up	I	GSENSOR_INT	G-Sensor interrupt input	PS2_CLK	
84	PS2_DATA/GPIO8_A1	I/O	up	I	COMPASS_INT	Compass interrupt input	PS2_DATA	
85	SC_DET/GPIO8_A2	I/O	up	I	GYR_INT	Gyroscope interrupt input	SC_DET	
86	SPI2_CSn1/SC_IO/GPIO8_A3	I/O	up	I	LIGHT_INT	Light sensor IC interrupt input	SC_IO	
87	I2C1_SDA/SC_RST/GPIO8_A4	I/O	up	I	I2C1_SDA_Sensor	I2C serial port 1,for Sensor,need external pull-up	SC_RST	
88	I2C1_SCL/SC_CLK/GPIO8_A5	I/O	up	I	I2C1_SCL_Sensor	I2C serial port 1,for Sensor,need external pull-up	SC_CLK	
89	SPI2_CLK/SC_IO_T1/GPIO8_A6	I/O	down	I	SPI2_CLK			
90	SPI2_CSn0/SC_DET_T1/GPIO8_A7	I/O	up	I	SPI2_CSn0			
91	SPI2_RXD/SC_RST_T1/GPIO8_B0	I/O	down	I	SPI2_RXD			
92	SPI2_TXD/SC_CLK_T1/GPIO8_B1	I/O	down	I	SPI2_TXD			
93	HOST_D0/TS_D0/CIF_D2/GPIO2_A0	I/O	down	I	CIF_D0	Camera data port	HSADC_D0	VCC18_DVP
94	HOST_D1/TS_D1/CIF_D3/GPIO2_A1	I/O	down	I	CIF_D1	Camera data port	HSADC_D1	
95	HOST_D2/TS_D2/CIF_D4/GPIO2_A2	I/O	down	I	CIF_D2	Camera data port	HSADC_D2	
96	HOST_D3/TS_D3/CIF_D5/GPIO2_A3	I/O	down	I	CIF_D3	Camera data port	HSADC_D3	
97	HOST_CKINP/TS_D4/CIF_D6/GPIO2_A4	I/O	down	I	CIF_D4	Camera data port	HSADC_D4	
98	HOST_CKINN/TS_D5/CIF_D7/GPIO2_A5	I/O	down	I	CIF_D5	Camera data port	HSADC_D5	
99	HOST_D4/TS_D6/CIF_D8/GPIO2_A6	I/O	down	I	CIF_D6	Camera data port	HSADC_D6	
100	HOST_D5/TS_D7/CIF_D9/GPIO2_A7	I/O	down	I	CIF_D7	Camera data port	HSADC_D7	
101	HOST_D6/TS_SYNC/CIF_VSYNC/GPIO2_B0	I/O	down	I	CIF_VSYNC	Camera vsync input	TS_SYNC	

102	HOST_D7/TS_VALID/CIF_HREF/GPIO2_B1	I/O	down	I	CIF_HREF	Camera href input	TS_VALID	
103	HOST_WKACK/GPS_CLK/TS_CLKOUT/CIF_CLKIN/GPIO2	I/O	down	I	CIF_CLKI	Camera clock input	TS_CLKOUT	
104	HOST_WKREQ/TS_FAIL/CIF_CLKOUT/GPIO2_B3	I/O	down	I	CIF_CLKO	Camera clock output	TS_FAIL	
105	CIF_D10/GPIO2_B6	I/O	down	I	CIF_RST0	Camera reset output for front	TV_RST	
106	CIF_D11/GPIO2_B7	I/O	down	I	CIF_RST1	Camera reset output for rear		
107	CIF_D0/GPIO2_B4	I/O	down	I	CIF_PDN0	Camera power down control output for front	TV_PWR	
108	CIF_D1/GPIO2_B5	I/O	down	I	CIF_PDN1	Camera power down control output for rear		
109	WIFI_ANT	O			WIFI_ANT	WIFI_ANT		
110	GND	G			GND			
111	I2C3_SCL/GPIO2_C0	I/O	up	I	I2C3_SCL	I2C serial port 3,for camera,need external pull-up		VCC18_DVP
112	I2C3_SDA/GPIO2_C1	I/O	up	I	I2C3_SDA	I2C serial port 3,for camera,need external pull-up		
113	GND	G			GND			
114	VCCA_CODEC	P			VCCA_CODEC	VCCA_CODEC power input (1.8-3.3V)		
115	VCCIO_CODEC	P			VCCIO_CODEC	VCCIO_CODEC power output (3.3V)		
116	SPDIF_TX/GPIO6_B3	I/O	down	I	SPDIF_TX	HDMI Digital audio optical output		VCCIO_CODEC
117	I2C2_SCL/GPIO6_B2	I/O	up	I	I2C2_SCL_AUDIO	I2C serial port 2,for Audio,need external pull-up		
118	I2C2_SDA/GPIO6_B1	I/O	up	I	I2C2_SDA_AUDIO	I2C serial port 2,for Audio,need external pull-up		
119	I2S_CLK/GPIO6_B0	I/O	down	I	I2S_CLK	I2S port, for audio part		
120	I2S_SDO3/GPIO6_A7	I/O	down	I	I2S_SDO3	I2S port, for audio part		
121	I2S_SDO2/GPIO6_A6	I/O	down	I	I2S_SDO2	I2S port, for audio part		
122	I2S_SDO1/GPIO6_A5	I/O	down	I	I2S_SDO1	I2S port, for audio part		
123	I2S_SDO0/GPIO6_A4	I/O	down	I	I2S_SDO0	I2S port, for audio part		
124	I2S_SDI/GPIO6_A3	I/O	down	I	I2S_SDI	I2S port, for audio part		
125	I2S_LRCK_TX/GPIO6_A2	I/O	down	I	I2S_LRCK_TX	I2S port, for audio part		
126	I2S_LRCK_RX/GPIO6_A1	I/O	down	I	I2S_LRCK_RX	I2S port, for audio part		
127	I2S_SCLK/GPIO6_A0	I/O	down	I	I2S_SCLK	I2S port, for audio part		
128	GND	G			GND			
129	VCCIO_RF	P			VCCIO_RF	VCCA_CODEC power input (1.8-3.3V)		

130	TS0_ERR/GPIO5_C3	I/O	down	I	3G_REG_ON	3G module internal regulators power enable output		VCCIO_RF
131	SPI0_CSn1/TS0_SYNC/GPIO5_C0	I/O	up	I	BP_RDY	BP ready status input		
132	SPI0_RXD/UART4_RX/TS0_D7/GPIO5_B7	I/O	up	I	AP_RDY	AP ready status output		
133	SPI0_TXD/UART4_TX/TS0_D6/GPIO5_B6	I/O	down	I	3G_DISABLE	3G module disable output		
134	SPI0_CSn0/UART4_RTSn/TS0_D5/GPIO5_B5	I/O	up	I	3G_WAKEUP_OUT	3G module wakeup CPU		
135	SPI0_CLK/UART4_CTSn/TS0_D4/GPIO5_B4	I/O	up	I	3G_WAKEUP_IN	CPU wakeup 3G module		
136	UART1_RTSn/TS0_D3/GPIO5_B3	I/O	up	I	UART1_RTSn	UART1 serial port, for 3G module		
137	UART1_CTSn/TS0_D2/GPIO5_B2	I/O	up	I	UART1_CTSn	UART1 serial port, for 3G module		
138	UART1_TX/TS0_D1/GPIO5_B1	I/O	down	I	UART1_TXD	UART1 serial port, for 3G module		
139	UART1_RX/TS0_D0/GPIO5_B0	I/O	up	I	UART1_RXD	UART1 serial port, for 3G module		
140	GND	G			GND			
141	VCC_LAN	P			VCC_LAN	VCC_LAN power input (1.8-3.3V)		
142	HOST_D15/MAC_TXCLK/SDIO1_PWREN/FLASH1_CSn2/GPIO4_B1	I/O	up	I	MAC_TXCLK	MAC transmit clock	FLASH1_CSn2	VCC_LAN
143	HOST_D14/MAC_COL/FLASH1_DQS/FLASH1_CSn3/GPIO4_B0	I/O	up	I	MAC_COL	MAC collision detect	FLASH1_DQS	
144	HOST_D13/MAC_CRS/SDIO1_CLKOUT/FLASH1_CSn1/GPIO4_A7	I/O	up	I	MAC_CRS	MAC carrier sense detect	FLASH1_CSn1	
145	HOST_D12/MAC_RXCLK/SDIO1_CMD/FLASH1_CSn0/GPIO4_A6	I/O	up	I	MAC_RXCLK	MAC receive clock	FLASH1_CSn0	
146	HOST_D11/MAC_MDIO/FLASH1_WRN/GPIO4_A5	I/O	up	I	MAC_MDIO	MAC management command and data	FLASH1_WRN	
147	HOST_D10/MAC_TXEN/FLASH0_CSn7/FLASH1_CLE/GPIO4_A4	I/O	up	I	MAC_TXEN	MAC transmit enable	FLASH1_CLE	
148	HOST_D9/MAC_CLK/FLASH0_CSn6/FLASH1_ALE/GPIO4_ A3	I/O	up	I	MAC_MCLK	MAC reference clock output	FLASH1_ALE	

149	HOST_D8/MAC_RXER/FLASH0_CSn5/FLASH1_RDN/GPIO4_A2	I/O	up	I	MAC_RXER	MAC receive error	FLASH1_RDN	
150	HOST_CKOUTN/MAC_RXDV/FLASH0_CSn4/FLASH1_WP/GPIO4_A1	I/O	up	I	MAC_RXDV	MAC receive data valid	FLASH1_WP	
151	HOST_CKOUTP/MAC_MDC/FLASH1_RDY/GPIO4_A0	I/O	up	I	MAC_MDC	MAC management clock	FLASH1_RDY	
152	GND	G			GND			
153	HOST_D7/MAC_RXD1/SDIO1_INTn/FLASH1_D7/GPIO3_D 7	I/O	up	I	MAC_RXD1	MAC receive data	FLASH1_D7	VCC_LAN
154	HOST_D6/MAC_RXD0/SDIO1_BKPWR/FLASH1_D6/GPIO3_D6	I/O	up	I	MAC_RXD0	MAC receive data	FLASH1_D6	
155	HOST_D5/MAC_TXD1/SDIO1_WRPRT/FLASH1_D5/GPIO3_D5	I/O	up	I	MAC_TXD1	MAC transmit data	FLASH1_D5	
156	HOST_D4/MAC_TXD0/SDIO1_DET/FLASH1_D4/GPIO3_D	I/O	up	I	MAC_TXD0	MAC transfer data	FLASH1_D4	
157	HOST_D3/MAC_RXD3/SDIO1_D3/FLASH1_D3/GPIO3_D3	I/O	up	I	MAC_RXD3	MAC receive data	FLASH1_D3	
158	HOST_D2/MAC_RXD2/SDIO1_D2/FLASH1_D2/GPIO3_D2	I/O	up	I	MAC_RXD2	MAC receive data	FLASH1_D2	
159	HOST_D1/MAC_TXD3/SDIO1_D1/FLASH1_D1/GPIO3_D1	I/O	up	I	MAC_TXD3	MAC transmit data	FLASH1_D1	
160	HOST_D0/MAC_TXD2/SDIO1_D0/FLASH1_D0/GPIO3_D0	I/O	up	I	MAC_TXD2	MAC transmit data	FLASH1_D0	
161	GND	G			GND			
162	SDMMC0_DET/GPIO6_C6	I/O	up	I	SDMMC0_DET	SDMMC0 detect input		SDMMC0
163	SDMMC0_CMD/GPIO6_C5	I/O	up	I	SDMMC0_CMD	SDMMC0 command output		
164	JTAG_TDO/SDMMC0_CLKOUT/GPIO6_C4	O	down	O	SDMMC0_CLKO	SDMMC0 clock output	TDO	
165	JTAG_TCK/SDMMC0_D3/GPIO6_C3	I/O	up	I	SDMMC0_D3	SDMMC0 data port	TCK	
166	JTAG_TDI/SDMMC0_D2/GPIO6_C2	I/O	up	I	SDMMC0_D2	SDMMC0 data port	TDI	
167	JTAG_TRSTn/SDMMC0_D1/GPIO6_C1	I/O	up	I	SDMMC0_D1	SDMMC0 data port	TRSTN	
168	JTAG_TMS/SDMMC0_D0/GPIO6_C0	I/O	up	I	SDMMC0_D0	SDMMC0 data port	TMS	
169	GND	G			GND			

170	eDP_TX0P	A			eDP_TX0P	eDP differential lane 0 positive output		EDP
171	eDP_TX0N	A			eDP_TX0N	eDP differential lane 0 negative output		
172	eDP_TX1P	A			eDP_TX1P	eDP differential lane 1 positive output		
173	eDP_TX1N	A			eDP_TX1N	eDP differential lane 1 negative output		
174	eDP_TX2P	A			eDP_TX2P	eDP differential lane 2 positive output		
175	eDP_TX2N	A			eDP_TX2N	eDP differential lane 2 negative output		
176	eDP_TX3P	A			eDP_TX3P	eDP differential lane 3 positive output		
177	eDP_TX3N	A			eDP_TX3N	eDP differential lane 3 negative output		
178	eDP_AXUN	A			eDP_AXUN	eDP differential AUX channel negative output		
179	eDP_AXUP	A			eDP_AXUP	eDP differential AUX channel positive output		
180	eDP_HOTPLUG /GPIO7_B3	I/O	down	I	SDMMC_PWR	SDMMC0 power control output		VCCIO_ PMU
181	GND	G			GND			
182	HDMI_HPD	A			HDMI_HPD	HDMI Hot Plug Detection interrupt		VCCIO_ PMU
183	I2C5_SDA/EDP HDMI_I2C_SDA/ GPIO7_C3	I/O	up	I	I2C5_SDA_HD MI	I2C serial port 5,for eDP and HDMI,need external pull-up		
184	I2C5_SCL/EDP HDMI_I2C_SCL/ GPIO7_C4	I/O	up	I	I2C5_SCL_HDM I	I2C serial port 5,for eDP and HDMI,need external pull-up		
185	ISP_FLASHTRI GIN/EDPHDMI_ CEC_T1/GPIO7 _C0	I/O	up	I	HDMI_CEC	headphone insert detect input		
186	HDMI_TXCP	A			HDMI_TXCP	HDMI differential pixel clock positive		HDMI
187	HDMI_TXCN	A			HDMI_TXCN	HDMI differential pixel clock negative		
188	HDMI_TX0P	A			HDMI_TX0P	HDMI channel 0 differential serial data positive		
189	HDMI_TX0N	A			HDMI_TX0N	HDMI channel 0 differential serial data negative		
190	HDMI_TX1P	A			HDMI_TX1P	HDMI channel 1 differential serial data positive		
191	HDMI_TX1N	A			HDMI_TX1N	HDMI channel 1 differential serial data negative		
192	HDMI_TX2P	A			HDMI_TX2P	HDMI channel 2 differential serial data positive		
193	HDMI_TX2N	A			HDMI_TX2N	HDMI channel 2 differential serial data negative		
194	GND	G			GND			

195	MIPI_TX/RX_D0P	A			MIPI_TX/RX_D0P	MIPI-DSI/CSI differential lane 0 positive		MIPI_TX/RX
196	MIPI_TX/RX_D0N	A			MIPI_TX/RX_D0N	MIPI-DSI/CSI differential lane 0 negative		
197	MIPI_TX/RX_D1P	A			MIPI_TX/RX_D1P	MIPI-DSI/CSI differential lane 1 positive		
198	MIPI_TX/RX_D1N	A			MIPI_TX/RX_D1N	MIPI-DSI/CSI differential lane 1 negative		
199	MIPI_TX/RX_CLKP	A			MIPI_TX/RX_CLKP	MIPI-DSI/CSI differential clock lane positive		
200	MIPI_TX/RX_CLKN	A			MIPI_TX/RX_CLKN	MIPI-DSI/CSI differential clock lane negative		
201	MIPI_TX/RX_D2P	A			MIPI_TX/RX_D2P	MIPI-DSI/CSI differential lane 2 positive		
202	MIPI_TX/RX_D2N	A			MIPI_TX/RX_D2N	MIPI-DSI/CSI differential lane 2 negative		
203	MIPI_TX/RX_D3P	A			MIPI_TX/RX_D3P	MIPI-DSI/CSI differential lane 3 positive		
204	MIPI_TX/RX_D3N	A			MIPI_TX/RX_D3N	MIPI-DSI/CSI differential lane 3 negative		
205	GND	G			GND			
206	MIPI_RX_D0P	A			MIPI_RX_D0P	MIPI-CSI differential lane 0 positive		VCC18_DVP
207	MIPI_RX_D0N	A			MIPI_RX_D0N	MIPI-CSI differential lane 0 negative		
208	MIPI_RX_D1P	A			MIPI_RX_D1P	MIPI-CSI differential lane 1 positive		
209	MIPI_RX_D1N	A			MIPI_RX_D1N	MIPI-CSI differential lane 1 negative		
210	MIPI_RX_CLKP	A			MIPI_RX_CLKP	MIPI-CSI differential clock lane positive		
211	MIPI_RX_CLKN	A			MIPI_RX_CLKN	MIPI-CSI differential clock lane negative		
212	MIPI_RX_D2P	A			MIPI_RX_D2P	MIPI-CSI differential lane 2 positive		
213	MIPI_RX_D2N	A			MIPI_RX_D2N	MIPI-CSI differential lane 2 negative		
214	MIPI_RX_D3P	A			MIPI_RX_D3P	MIPI-CSI differential lane 3 positive		
215	MIPI_RX_D3N	A			MIPI_RX_D3N	MIPI-CSI differential lane 3 negative		
216	VCC18_DVP	P			VCC18_DVP	VCC18_DVP power input (1.8V)		

4. 模块外观图

5. PCB 结构尺寸

PCBA 板厚度 2.5mm，长宽：61*61MM

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